

b) first coding step of outputting N bits data by coding the first digital information signal, the N representing an integer not less than 2;

c) second coding step of outputting M bits data by coding the second digital information signal, the M representing an integer other than the N;

d) converting step of converting the N bits data output in said first coding step, into M bits data; and

e) an adding step of adding an error correction code to the M-bit data wherein

said adding means receives selectively the M-bit data from said second coding means or the M-bit data from said converting means and performs a common addition processing irrespective of the M-bit data from the second coding means and the M-bit data from said converting means. --.

REMARKS

Claims 11-21 have been cancelled and claims 22-30 have been added.

The Examiner has rejected applicants' claims 13 and 15-16 under 35 USC § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one of skill in the art to make and use the invention. In particular, the Examiner states that the

specification does not describe the predictive coding circuits recited in these claims.

As above-indicated, claims 13 and 15-16 have been deleted. Moreover, newly added claims 22-30 do not recite predictive coding circuits. Accordingly, the Examiner's rejection in this regard has been obviated.

The Examiner has rejected applicants' claims 11, 13 and 19 under 35 USC § 102(e) as anticipated by the Yoshimura, et al. patent. Claim 12 and 14-18 have been rejected under 35 USC § 103(a) as unpatentable over the Yoshimura, et al. patent taken in view of FIG. 1 of applicants' drawings and the related description in applicants' specification. Finally, claims 20 and 21 have been rejected under 35 USC § 103(a) as unpatentable over the Yoshimura, et al. patent taken in view of the Examiner's Official Notice.

Applicants' claims 11-21 have been cancelled, thereby obviating these rejections. Moreover, to the extent the Examiner believes that the Examiner's rejections are applicable to newly added 22-30, they are respectfully traversed.

Applicants' newly added independent claims 22 and 30 are directed to a digital signal encoding apparatus and method in which a first or second digital information signal is input. The first digital information signal is coded by outputting N bits of data, where N is an integer greater than one. The

second digital information signal is coded by outputting M bits of data, where M is an integer other than N. The N bits of data for coding the first information signal are then converted into M bits of data.

An error correction code is then added to the M bit data. The adding occurs selectively for the M bit data converted from the N bit data or for the data coded as M bit data and a common addition processing is used irrespective of the particular M bit data, i.e., whether it is the converted M bit data or the coded M bit data..

Such a construction is not taught or suggested by the cited art of record. More particularly, in the Yoshimura, et al. patent the audio and video signals are subjected to individual error correction coding. This is clearly seen from FIG. 7 of the patent. Thus, there is no teaching or suggestion in the patent of an error correction coding being added with common addition processing to encoded M bit data or converted M bit data, as required by applicants' independent claims 22 and 30.

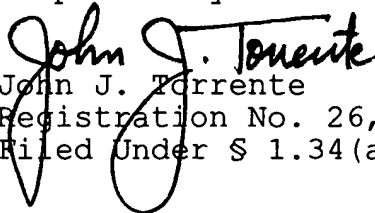
Such claims, and their respective dependent claims are thus believed to patentably distinguish over the Yoshimura, et al. patent. Moreover, applicants' FIG. 1 and the related description in applicants' specification and the Examiner's

Official Notice add nothing to the Yoshimura, et al. patent to change this conclusion.

In view of the above, it is submitted that applicants' claims, as amended, patentably distinguish over the cited art of record. Accordingly, reconsideration of the claims is respectfully requested.

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